REMARKS

In the Official Action mailed 8 January 2007, the Examiner withdrew the finality of the previous Office action and set forth new §103(a) rejections in light of the amendment entered 30 October 2006. The Examiner reviewed claims 1-33 and has rejected claims 1-33 under 35 U.S.C. §103(a).

Claims 1-33 remain pending.

Rejection of Claims 1-33 under 35 U.S.C. §103(a)

The Examiner has rejected claims 1-33 under 35 U.S.C. §103(a) as being unpatentable over Bartkowiak et al. (US 5771362) (hereinafter referred to as "Bartkowiak") in view of Wang et al. (US 7028134) (hereinafter referred to as "Wang"). Applicant respectfully requests reconsideration.

For at least the reasons stated below, Applicant asserts that Bartkowiak in view of Wang fails to teach or suggest all the limitations of the claims in the present application, and that the Examiner does not present a reasonable basis for motivation to combine Bartkowiak and Wang and then to further modify the combination, to produce the claimed invention.

For context, Applicant provides a brief review of Bartkowiak and Wang. Then, Applicant addresses the rejection specifically.

Bartkowiak -

Bartkowiak discloses that, "[b]roadly speaking, the present invention contemplates a processor comprising an instruction sequencer and a bus interconnect. The instruction sequencer is configured to execute instructions having an opcode field and a bus configuration field" (Bartkowiak, col. 2 lines 42-45). Bartkowiak further describes that "the bus interconnect 28 is configurable to transfer data between a particular source and one or more destinations according to the execution of an instruction within instruction sequencer 16" (Bartkowiak, col. 4: lines 11-14). Bartkowiak further describes the operation of the interconnect (a single routing unit) in column 4, lines 23-32 which are reproduced below:

> Bus interconnect **28** receives control signals upon an interconnect control bus **30** from instruction sequencer **16**. Instruction sequencer **16** asserts a particular control signal to cause transfer of data between a particular source and a particular destination. Deasserting the particular control signal inhibits transfer of data between the particular source and the particular destination. While the particular control signal is deasserted, a second control signal may be asserted to cause transfer of data from another source to the particular destination. The control signals upon interconnect control

As can be seen in the above reproduced section and also in Figure 1 of Bartkowiak, Bartkowiak discloses establishing a route for a cycle by the instruction sequencer supplying a first control signal to the bus interconnect (single routing unit), the sequencer deasserting the control signal to the bus interconnect (single routing unit), and the sequencer then supplying a second control signal to the bus interconnect (single routing unit). Thus, Bartkowiak discloses a single routing unit and supplying control signals serially to configure the single routing unit within each cycle to establish a route among the functional units.

Bartkowiak does not disclose a plurality of routing units, and therefore necessarily Bartkowiak thus does not disclose supplying control signals in parallel from the sequencer to a plurality of routing units to establish a route for a cycle. Furthermore, Bartkowiak does not disclose routing units being coupled to respective subsets of functional units.

Wang-

Wang describes a single communication device including a plurality of crossbar circuits receiving communication signals and a clock signal over parallel channels from a communication processing circuit (See Wang, Figure 3 and col. 4 lines 42-47). Wang describes prior art in which "[a]n individual serial channel transfers communications in a single stream of bits" (Wang, col. 2, lines 17-18). Wang describes that the prior art using serial channels needs a clock encoding and a clock recovery circuit for each serial channel and that "the clock encoding and recovery circuitry requires excessive power and space" (Wang, col. 4 lines 29-31). Wang discloses that an advantage of his invention over the prior art is that "[t]he clock circuitry for the parallel channels is simpler than that for serial channels. The clock circuitry for a parallel channel is shared by all of the data signals within the parallel channel. Advantageously, the

simplification and sharing of the clock circuitry reduces the amount of power and physical space that is required to provide synchronized clocking. The power and space savings can be used to support higher speed communication devices." (Wang, col.2 line 65 to col.3 line 6).

Wang further describes that "[i]n response to control signals from communication processing circuitry 301, crossbar integrated circuits 302-304 switch the communications from incoming parallel channels 312-314 to the proper outgoing parallel channels 315-317" (Wang, col. 4 lines 23-27). Thus, Wang discloses the communication processing circuitry supplying the control signals to the crossbar integrated circuits. However, Wang does not disclose the manner in which the control signals are supplied.

Wang does not disclose control word distribution circuitry which supplies the routing control signals in parallel to the plurality of routing units. Further, Wang does not disclose routing units being coupled to respective subsets of functional units.

Independent Claim 1:

Independent claim 1 reads as follows:

1. A data processing system, comprising:

a plurality of functional units having respective inputs and outputs, and adapted to perform respective tasks using input data at the respective inputs and to supply output data at the respective outputs, within a cycle;

a plurality of routing units, responsive to respective routing control signals, by which data is steered among inputs and outputs of the plurality of functional units, routing units in the plurality of routing units being coupled to respective subsets of functional units in the plurality of functional units, wherein at least one of said respective subsets is different than another of said respective subsets; and

control word distribution circuitry which supplies the routing control signals in parallel to the plurality of routing units to establish a route for a cycle, where the route includes applying data output in the cycle by a first functional unit in the plurality of functional units as input in the cycle to a second functional unit in the plurality of functional units, and applying data output by the second functional unit in the cycle as input in the cycle to a third functional unit in the cycle.

The Examiner takes the position that Bartkowiak teaches all the limitations of claim 1 with the exception of a plurality of routing units. Office Action, page 3. Applicant points out that in addition, Bartkowiak does not teach the claimed "control word distribution circuitry which supplies the routing control signals in parallel..." as recited in claim 1. The Examiner takes the mistaken position that the "control word distribution circuitry ..." in claim 1 reads on column 2, lines 15-32 of Bartowiak. However, this passage discusses a dynamically configurable interconnect only. It does not describe any structure corresponding to the claimed control word distribution circuitry. In fact, and unlike the claim, Bartkowiak describes a system that supplies the control words for the dynamically configurable interconnect in series. See, column 2, lines 53-62 of Bartkowiak.

Furthermore, Applicant points out that Bartkowiak does not describe even a single routing unit that is coupled to a "subset" of the functional units as required in the claim. Rather, the dynamic interconnect of Bartkowiak is coupled to all the functional units in the system, rather than to a subset of functional units as required in the claim.

Therefore, in a detailed review of Bartkowiak, one finds that it does not describe or suggest at least three limitations in claim 1.

The Examiner relies on Wang to teach the plurality of routing units of claim 1. Wang in fact describes a single routing unit having a single input channel 311 and a single output channel 318, and which comprises a plurality of crossbar switches configured for routing data between the input channel 311 and output channel 318 channels in a high speed communication system. See, Wang, column 4, line 13-41. The links 311 and 318 operate according to a communications protocols, such as SONET, ATM, IP, CDMA and Ethernet. Wang, column 4, lines 5-13. The routing control signals according to these protocols are not described in Wang. Applicant believes that the routing control signals are carried by the communication protocol overhead associated with data being routed. The crossbar switches in Wang switch the data signals among data channels "as directed by communication processing circuitry 301." See, Wang, column 5, lines 36-49. There is no discussion in Wang about how such directions are provided to the crossbar switches, and no structures are shown to accomplish this transfer. Therefore, one could presume that the control signals for the crossbar switches are provided in series with the data on the parallel channels. However, the Office Action does not address this issue. Therefore, the prima facie case is incomplete in this respect.

Furthermore, even if Wang did suggest supplying routing control signals in parallel to crossbar switches in a communications device, it does not describe even a single routing unit that is coupled to a "subset" of the functional units in the system, as required in claim 1. First, there is no functional unit in Wang other than the communication processing circuitry 301. All crossbars in Wang take their input from and supply their output to the same communication processing circuitry 301. If the Examiner takes the position that the "plurality of functional units" of claim 1 reads on the plurality of parallel channels 511-516 on the communication processing circuitry 501 of Figure 5 in Wang, then the same issue arises. All of the crossbar switches are coupled to all of the parallel channels. There is no switch coupled to a subset of the channels.

Accordingly, even if Bartkowiak were modified by replacing the dynamic bus interconnect 28 with a plurality of crossbar switches as shown in Wang, the claimed architecture does not result.

Therefore, Applicant submits that the claimed invention would not result from a combination of Bartkowiak and Wang.

Further, the Examiner states that it "would have been obvious to one or ordinary skill in the art at the time of the invention to apply the teachings of Wang for the benefit of Bartkowiak, because to do so allowed a system designer to reduce power consumption and footprint required to provide synchronized clocking, as taught by Wang in col. 3 lines 1-6." (Office Action, page 4).

However, Bartkowiak's interconnect is configured by the sequencer asserting and deasserting control signals. There is no clock signal being supplied to the interconnect (see Bartkowiak Figures 1, 2 and 3A-3C). Thus, the person of ordinary skill would not look to Wang to improve the system of Bartkowiak for the reason suggested in the Office Action, because Bartkowiak does not include synchronized clocking and does not suffer the problem solved by Wang. Therefore, the Office Action does not include a convincing line of reasoning as to why a person skilled in the art would have found the claimed invention to have been obvious in light of the teachings of the Bartkowiak and Wang.

In summary, Applicant submits that the combination of Bartkowiak and Wang does not provide the claimed plurality of routing units coupled to "respective subsets" of the plurality of functional units, and does not provide the claimed control word distribution circuitry.

Furthermore, Applicant submits that no reasonable basis for combining or modifying the references has been provided that leads to the invention recited in claim 1.

Therefore, for at least the reason cited above, the *prima facie* case of obviousness is incomplete and independent claim 1 is patentably distinct from Bartkowiak in view of Wang.

Independent Claims 12, 23, and 29:

Independent claims 12, 23, and 29 each include at least some of the limitations cited above with respect to claim 1. Additionally, in the rejection of independent claims 12, 23, and 29 the Examiner has relied upon the same motivation to combine Bartkowiak and Wang as the Examiner gave for independent claim 1. Therefore, for at least the reasons cited above with respect to claim 1, the prima facie case of obviousness is incomplete and independent claims 12, 23, and 29 are patentably distinct from Bartkowiak in view of Wang.

Dependent Claims:

Claims 2-11, 13-22, 24-28, and 30-33 depend ultimately from one of independent claims 1, 12, 23, and 29. It is submitted that these claims also add their own limitations which render them patentable in their own right. Applicant has reviewed the grounds on which these claims were rejected in the Office Action and respectfully does not agree with them. However, Applicant does not believe it necessary to argue these points at this time because of the allowability of the independent claims. Applicant reserves the right to argue these points should it become necessary in the future.

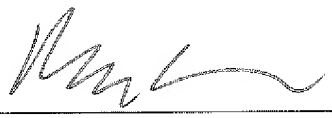
Accordingly, reconsideration of the rejection of claims 1-33 is respectfully requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (UNMI 1000-1).

Respectfully submitted,



Dated: 9 April 2007

Mark A. Haynes, Reg. No. 30,846

HAYNES BEFFEL & WOLFELD LLP
P.O. Box 366
Half Moon Bay, CA 94019
(650) 712-0340 phone
(650) 712-0263 fax